REMARKS

The Examiner has rejected Claims 1, 3-8, and 32 under 35 U.S.C. 103(a) as being unpatentable over Harriman et al. (U.S. Patent No. 5,898,687), in view of Turner et al. (U.S. Patent No. 7,106,693). The Examiner has rejected Claims 9 and 11-12 under 35 U.S.C. 103(a) as being unpatentable over Harriman et al. (U.S. Patent No. 5,898,687), in view of Turner et al. (U.S. Patent No. 7,106,693), and in further view of Hebb et al. (U.S. Patent No. 6,711,153). The Examiner has rejected Claims 15, 17-21, 24-27, and 29-31 under 35 U.S.C. 103(a) as being unpatentable over Harriman et al. (U.S. Patent No. 5,898,687), in view of Turner et al. (U.S. Patent No. 7,106,693), and in further view of Raza et al. (U.S. Patent No. 7,016,349). The Examiner has rejected Claims 22 and 28 under 35 U.S.C. 103(a) as being unpatentable over Raza et al. (U.S. Patent No. 7,016,349), in view of Turner et al. (U.S. Patent No. 7,106,693). Applicant respectfully disagrees with such rejection, especially in view of the amendments made hereinabove to the independent claims. Specifically, applicant has amended the independent claims to at least substantially include the subject matter of former dependent Claim 14.

With respect to independent Claims 1 and 31, the Examiner has relied on items 332-338 of Figure 3, and Col. 7, lines 30-32 from Harriman to make a prior art showing of applicant's claimed "port transmit controller coupled to the first and second data structures and configured to provide a second sequence of packet pointers" (see this or similar, but not necessarily identical language in the aforementioned independent claims).

Applicant respectfully asserts that items 332-338 of Figure 3 from Harriman merely show 'independent round robin (RR) subarbiter circuits 332-338 which, in the illustrative embodiment, are 2-state selectors that "skew" selection of the cell at each priority level' (Col. 7, lines 29-32 – emphasis added). However, simply disclosing 'independent round robin (RR) subarbiter circuits 332-338 which...are 2-state selectors that "skew" selection of the cell at each priority level' (emphasis added), as in Harriman, fails to even suggest "a port transmit controller coupled to the first and second data structures and configured to provide a second sequence of packet pointers" (emphasis added), as claimed by applicant.

With respect to independent Claim 9, the Examiner has relied on item 80 of Figure 3 from Hebb to make a prior art showing of applicant's claimed "third data structure embodied on a tangible computer readable medium coupled to the second data structure and configured to store a plurality of status flags."

Applicant respectfully asserts that item 80 of Figure 3 from Hebb merely shows "Control/Status registers." However, simply disclosing "Control/Status registers," as in Hebb, fails to teach or suggest "a third data structure embodied on a tangible computer readable medium coupled to the second data structure and configured to store a plurality of status flags" (emphasis added), as claimed by applicant.

With respect to independent Claims 15 and 21, the Examiner has relied on the system 400 from Figure 13 and Col. 14, lines 27-29 from Raza to make a prior art showing of applicant's claimed "if the overall tail is the second type, setting an overall tail flag to a first state, and setting an entry to the first state" and "if the overall tail is the first type, adding the pointer to the second data structure field with the first state" (see this or similar, but not necessarily identical language in the aforementioned independent claims).

Applicant respectfully asserts that, in Col. 14, lines 27-29, Raza merely teaches that "the system 400 may allow a multicast queue to send a single location and unicast queue to implement complex processing" (emphasis added). However, simply disclosing that "the system 400 may allow a multicast queue to send a single location and unicast queue to implement complex processing" (emphasis added), as in Raza, fails to even suggest, "if the overall tail is the second type, **setting** an overall tail flag to a first state, and setting an entry to the first state" (emphasis added), as claimed by applicant.

Further, disclosing that "the system 400 may allow a multicast queue to send a single location and unicast queue to implement complex processing" (emphasis added), as in Raza, fails to even suggest, "if the overall tail is the first type, adding the pointer to

the second data structure field with the first state" (emphasis added), as claimed by applicant.

Still yet, with respect to independent Claims 15 and 21, the Examiner has relied on the system 400 from Figure 13 and Col. 14, lines 23-25 from Raza to make a prior art showing of applicant's claimed "if the overall tail is the second type, adding the pointer to a second data structure field with a second state" (see this or similar, but not necessarily identical language in the aforementioned independent claims).

Applicant respectfully asserts that, in Col. 14, lines 23-25, Raza merely teaches that "[t]he system 400 compris[es] a multicast pointer logic block configured to generate and store multicast addresses" (emphasis added). However, simply disclosing that "[t]he system 400 compris[es] a multicast pointer logic block configured to generate and store multicast addresses" (emphasis added), as in Raza, simply fails to teach "if the pointer is the second type and the overall tail is the second type, adding the pointer to the second data structure field with a second state" (emphasis added), as claimed by applicant.

Additionally, with respect to independent Claims 15 and 21, the Examiner has relied on the Col. 15, lines 2-3 from Raza to make a prior art showing of applicant's claimed "setting the first type tail to the pointer" and "setting the overall tail flag to the second state" (see this or similar, but not necessarily identical language in the aforementioned independent claims).

Applicant respectfully asserts that the excerpt from Raza relied upon by the Examiner simply teaches "the configuration logic 502 writes to the queue pointer memory 504." However, simply teaching that "the configuration logic 502 writes to the queue pointer memory 504" (emphasis added), as in Raza, fails to teach or even suggest "setting the first type tail to the pointer" (emphasis added) or "setting the overall tail flag to the second state" (emphasis added), as claimed by the applicant. Clearly, writing to "the queue pointer memory" (emphasis added), as in Raza, simply fails to suggest "setting the first type tail to the pointer" (emphasis added) or "setting the overall tail flag to the second state" (emphasis added), as claimed by the applicant.

Further, with respect to independent Claims 15 and 21, the Examiner has relied on the following excerpts from Raza to make a prior art showing of applicant's claimed "getting a first type tail" and "linking the pointer in a first data structure to the first type tail" (see this or similar, but not necessarily identical language in the aforementioned independent claims).

> "When writing data to a different queue, the write pointer (or tail pointer) may be fetched from the FIFO pointer memory 134 (also called the queue pointer memory)." (Col. 7, lines 9-12)
>
> "When a new queue address is requested for a read or write operation, the address logic block 130 generally requests the data from the pointer memory 134." (Col. 7, lines 29-32)

Applicant respectfully asserts that the excerpts from Raza relied upon by the Examiner simply teach that "[w]hen writing data to a different queue, the write pointer (or tail pointer) may be fetched from the FIFO pointer memory" (emphasis added). However, merely teaching that the "tail pointer ... may be fetched from the FIFO pointer memory" (emphasis added), as in Raza, fails to disclose "getting a first type tail" (emphasis added), as claimed by applicant. More specifically, Raza fails to teach "getting a first type tail," where the "overall tail is the second type" (emphasis added), as in the context claimed by applicant (see independent Claims 15 and 21 for context).

Furthermore, in Col. 7, lines 29-32, Raza simply teaches that "[w]hen a new queue address is requested for a read or write operation, the address logic block 130 generally requests the data from the pointer memory 134" (emphasis added). However, simply teaching that the "address logic block 130 ... requests ... data from pointer memory 134" (emphasis added) when a new queue address is requested, as in Raza, simply fails to disclose "linking the pointer in a first data structure to the first type tail" (emphasis added), as claimed by applicant. More specifically, Raza fails to teach "linking the pointer in a first data structure to the first type tail" (emphasis added) where the "overall tail is the second type" (emphasis added), as in the context claimed by applicant (see independent Claims 15 and 21 for context).

With respect to independent Claims 22, 28, and 29, the Examiner has relied on item 350 of Figure 3 from Turner to make a prior art showing of applicant's claimed "if the overall head is the first type... updating the first type head with a next pointer from a first data structure" (see this or similar, but not necessarily identical language in the aforementioned independent claims).

Applicant respectfully asserts that item 350 of Figure 3 from Turner merely shows "a data structure 350 which may be used to determine the next target time for sending information corresponding to an information stream" (Col. 7, lines 51-53). Furthermore, in Col. 7, lines 53-60, Turner teaches that "[d]ata structure 350 is an array having an index for each of the information streams 350" where "[f]or each information stream, a packet spacing value 361 is maintained which indicates an ideal time between sending packets which corresponds to the target pacing rate" and "[a] target time value 362 is maintained for each information stream 355 which indicates a current target time for sending a packet of the information stream 355" (emphasis added).

However, simply disclosing "a data structure 350 which may be used to determine the next target time for sending information corresponding to an information stream" and that "[a] target time value 362 is maintained for each information stream 355 which indicates a current target time for sending a packet of the information stream 355" (emphasis added), as in Turner, fails to even suggest that "if the overall head is the first type... updating the first type head with a next pointer from a first data structure" (emphasis added), as claimed by applicant.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the

prior art and not based on applicant's disclosure. *In re Vaeck*,947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the excerpts from the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above. Nevertheless, despite such paramount deficiencies and in the spirit of expediting the prosecution of the present application, applicant has incorporated the subject matter of former Claim 14 into the independent claims.

With respect to the subject matter of former Claim 14 (now at least substantially incorporated into the independent claims), the Examiner has rejected the same under 35 U.S.C. 103(a) as being unpatentable over Harriman et al. (U.S. Patent No. 5,898,687), in view of Turner et al. (U.S. Patent No. 7,106,693), in view of Hebb et al. (U.S. Patent No. 6,711,153), and in further view of Raza et al. (U.S. Patent No. 7,016,349). Specifically, the Examiner has relied on Col. 11, lines 14-15; Col. 11, lines 18-20; and Col. 14, lines 60-61 from Raza to make a prior art showing of applicant's claimed technique "wherein the plurality of status flags includes: a first type packet pointer head position indication; a first type packet pointer tail position indication; an overall head pointer indication; and an overall tail pointer indication" (see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully asserts that the excerpts from the Raza reference relied upon by the Examiner simply teach that "[t]he address generator circuit 402 may receive a signal (e.g., UNICAST_HTPR) from the logic block 404" (Col. 11, lines 14-15). Further, the excerpts teach that "[t]he signal UNICAST_HPTR may indicate a head pointer for unicast packets" and that "[t]he signal MULTICAST_HPTR may indicate a head pointer for multicast packets" (Col. 11, lines 18-20).

However, simply disclosing that "[t]he address generator circuit 402 may receive a signal (e.g., UNICAST_HTPR) from the logic block 404" where "[t]he signal UNICAST_HPTR may indicate a head pointer for unicast packets" (emphasis added), as

in Raza, simply fails to teach "the plurality of status flags includes...a first type packet pointer head position indication" or "an overall head pointer indication" (emphasis added), as claimed by applicant.

Furthermore, in Col. 14, lines 59-62, Raza merely teaches that "[t]he registers 508a-508n may be configured to store information such as the head pointer address, the tail pointer address, the depth of each queue and/or the length of each queue." However, simply teaching that "[t]he registers 508a-508n may be configured to store information such as...the tail pointer address" (emphasis added), as in Raza, simply fails to teach "a first type packet pointer tail position indication" (emphasis added), as claimed by applicant. Clearly, a "tail pointer address" (emphasis added), as in Raza, simply fails to teach a "packet pointer tail position indication" (emphasis added), as claimed by applicant.

Additionally, the Examiner has stated that "[w]hile Harriman'687, Turner'693, Hebb'153 and Raza'349 [do not] teach[ ] an overall tail pointer indication, said over[all] tail pointer indication is simply an alternative arrangement in the art" and "[i]t would have been obvious to one of ordinary skill in the art at the time of invention to modify Harriman'687, Turner'693 and Hebb'153's system to incorporate, as taught by Raza'349, that the plurality of status flags includes a first type packet pointer head position indication; a first type packet pointer tail position indication; an overall head pointer indication; and an overall tail pointer indication." The Examiner further argues that "[t]he motivation to combine these teachings is to enable an apparatus to extract in-band information or skip extraction and perform a look ahead operation (column 3, lines 13-17)."

Applicant respectfully disagrees and asserts that in Col. 3, lines 13-17, Raza merely teaches that "[a]nother aspect of the present invention concerns an apparatus configured to extract in-band information or skip extraction of the in-band information and perform a look ahead operation" where "[t]he apparatus may be configured to switch between the extraction and the skipping of the extraction" (emphasis added). However, simply disclosing "switch[ing] between the extraction and the skipping of the extraction"

(emphasis added), as in Raza, fails to even suggest "an overall tail pointer indication," as claimed by applicant. Accordingly, it cannot be said that "[i]t would have been obvious to one of ordinary skill in the art at the time of invention to modify Harriman'687, Turner'693 and Hebb'153's system to incorporate, as taught by Raza'349, that the plurality of status flags includes a first type packet pointer head position indication; a first type packet pointer tail position indication; an overall head pointer indication; and an overall tail pointer indication," as argued by the Examiner. Applicant thus formally requests a specific showing of the subject matter in ALL of the claims in any future action.

Applicant further notes that the prior art is also deficient with respect to the dependent claims. For example, with respect to dependent Claim 8, the Examiner has relied on Col. 7, lines 13-14 and Col. 2, lines 38-41 from Harriman to make a prior art showing of applicant's claimed technique "wherein...the packet controller is configured to provide ... each of the plurality of second type packet pointers to each of a group of the plurality of FIFO structures" (as amended).

Applicant respectfully asserts that the excerpts relied upon by the Examiner simply teach that "each port of the switch has a unicast/multicast output queue pair for each predetermined priority level" (Col. 7, lines 13-15 – emphasis added) and that "there is preferably one multicast output queue for each output port of the switch at each predetermined priority level" (Col. 2, lines 39-41 – emphasis added). However, merely teaching that "each port of the switch has a unicast/multicast output queue pair for each predetermined priority level" (emphasis added) and that "there is preferably one multicast output queue for each output port of the switch at each predetermined priority level" (emphasis added), as in Harriman, fails to disclose "the packet controller is configured to provide ... each of the plurality of second type packet pointers to each of a group of the plurality of FIFO structures" (emphasis added), as claimed by applicant.

With respect to dependent Claim 20, the Examiner has relied on Col. 15, lines 58-60 from Raza to make a prior art showing of applicant's claimed technique

"wherein...the first data structure is accessed at most once; and the second data structure is accessed at most once."

Applicant respectfully asserts that, in Col. 15, lines 58-60, Raza merely teaches that "the system 600 may allow each pointer to be written whenever a location is accessed (e.g., every eight cycles)." However, simply teaching that "the system 600 may allow each pointer to be written whenever a location is accessed" (emphasis added), as in Raza, simply fails to suggest applicant's claimed technique "wherein...the first data structure is accessed at most once; and the second data structure is accessed at most once" (emphasis added).

Again, applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above.

Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

Thus, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The

Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. RMI1P041).

Respectfully submitted,
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